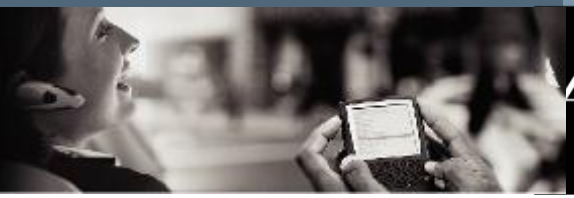
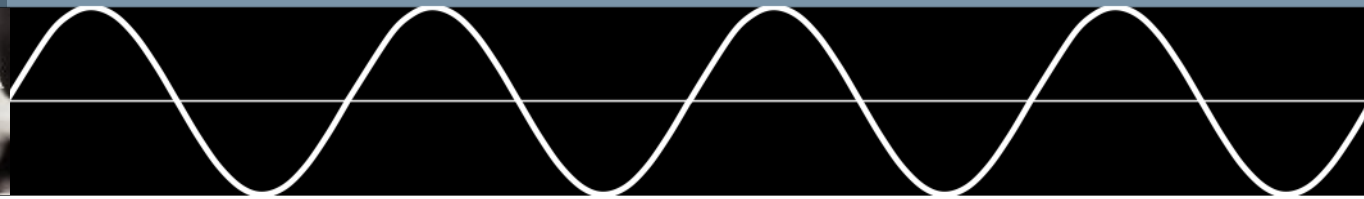
IEEE802.3bt
PSE and PD PI Specifications
Rev 1.0

J. Heath – Linear Technology





LINEAR TECHNOLOGY

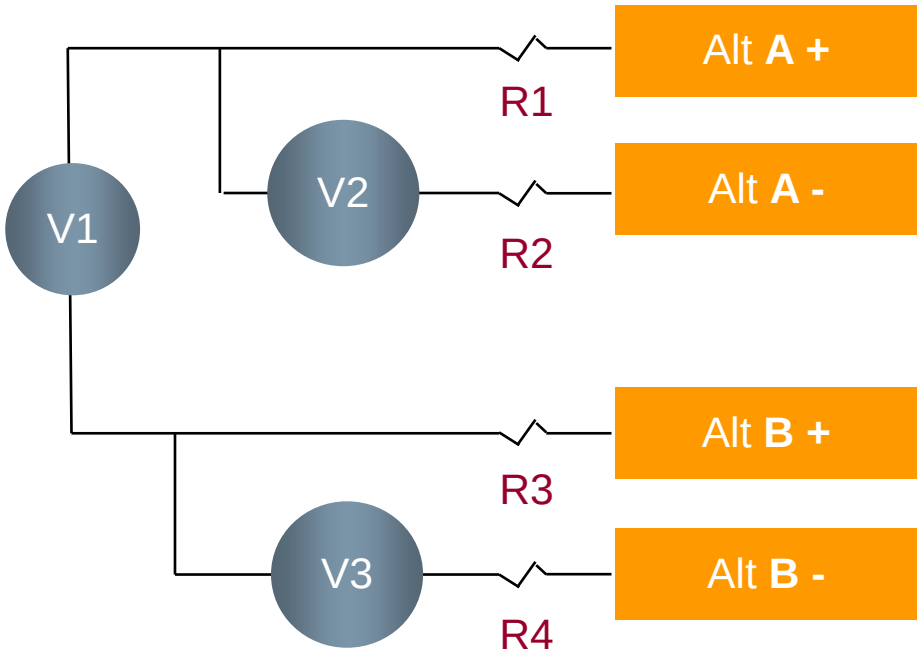
Supporters

Goal of this Presentation

- Provide a basis for discussion of the PSE and PD PI specification to facilitate a consensus for a motion in the ‘bt’ task force and creating imbalance specifications for the PSE and PD PI.
- Good work has been done and continues to be done in the Ad-Hoc based on likely PSE and PD configurations
- Some thinking on what other considerations as our attention turns to specifying a PI which is not implantation specific.

A Necessary and Sufficient PSE PI Model.

- **This is not an implementation centric model, it is a PSE PI centric model.**
- Thinking of a PSE PI without respect to implementation requires these parameters, or equivalent parameters to be specified to ensure interoperability with respect to current imbalance (and perhaps other important interoperability concerns) and safety concerns.
- For SELV, we know that any two of the four outputs (really 8 wires) must never be more than 60V (or 57 in IEEE PoE)
- In this model, a way to specify the PI:
  - R1, R2, R3, and R4 must have a matching specification
  - V1 must be below a specified voltage
  - V2 and V3 must be within a specified delta voltage
- It is certainly true that a low V2 can compensate for a higher R2 at some current, but creating a specification matrix for this can be
  - Difficult to understand
  - Difficult to test
- This model ignores the delta R in the magnetic and connector and PCB parasitics between them as we are talking about pair to pair imbalance. It may be a good idea to use 8 resistors and create rules to cover single pair imbalance but I am not currently advocating this.



LINEAR TECHNOLOGY

A Necessary and Sufficient PD PI Model.

- **This is not an implementation centric model, it is a PSE PI centric model.**
- Thinking of a PD PI without respect to implementation requires these parameters, or equivalent parameters to be specified to ensure interoperability with respect to current imbalance (and perhaps other important interoperability concerns).
- The PD is a power user so SELV is not a problem and may not source voltage/power
- In this model, a way to specify the PI:
  - R1, R2, R3, and R4 must have a matching specification
  - V1 - V2 must be within a specified delta voltage
  - V2 - V3 must be within a specified delta voltage
- It is certainly true that a low V2 can compensate for a higher R2 at some current, but creating a specification matrix for this can be
  - Difficult to understand
  - Difficult to test
- This model ignores the delta R in the magnetic and connector and PCB parasitics between them as we are talking about pair to pair imbalance. It may be a good idea to use 8 resistors and create rules to cover single pair imbalance but I am not currently advocating this.